Digital Dual Mixer Time Difference for Sub-Nanosecond Time Synchronization in Ethernet

Pedro Moreira
University College London
London, United Kingdom
pmoreira@ee.ucl.ac.uk

Pablo Alvarez
CERN
Geneva, Switzerland
pablo.alvarez@cern.ch

Javier Serrano
CERN
Geneva, Switzerland
javier.serrano@cern.ch

Izzat Darwezeh
University College London
London, United Kingdom
izzat.darwezeh@ee.ucl.ac.uk

Tomasz Wlostowski
CERN
Geneva, Switzerland
Tomasz.Wlostowski@cern.ch

Abstract— A digital architecture for the Dual Mixer Time Difference (DMTD) is presented. This architecture has several advantages over other phase frequency detectors such as being linear, not having a dead zone and with an accuracy within the sub-picoseconds range. The intrinsic phase noise present in all timing signals is the main cause of the limitation in the accuracy of this phase frequency detector. Therefore, this paper describes the advantages and disadvantages of the presented architecture as well as how its performance changes with the clock phase noise by showing some experimental measurements. The application of this architecture, for the use of Ethernet as both data and synchronization network, is also discussed.

I. INTRODUCTION

Many electronic communication systems require accurate frequency and time synchronization. However sub-nanosecond accuracies are only needed in few and specific applications. One of such application is found in the timing system of large scale physics accelerators as the ones located at CERN.

One of the elements needed to achieve sub-nanosecond accuracy in synchronization is a phase frequency detector. Several phase frequency detectors are proposed by researchers and many are available commercially. These devices can reach very high accuracy, however, they require the employment of either a very fast digital counter to measure the phase between clocks or the use of analog devices, such as charge-pumps, which introduce noise and limits the accuracy of the phase detector.

The most important and best known phase and frequency detector is shown in Fig. 1. It consists of a pair of D flip-flops plus an AND gate and a delay in a feedback connection. The inputs D of the flip-flops are held permanently high. One of the flip-flop's outputs is labeled UP and the other is labeled DOWN. A clock transition turns on its associated flip-flop. If UP and DOWN are high simultaneously, the output of the AND gate, will resets both flip-flops.

Some delay has to be added in series with the CLR signal. The transitions in both flip-flops are necessary not coincident, due to the expected difference in the frequencies of the two clocks, and therefore the delay has to be added to increase
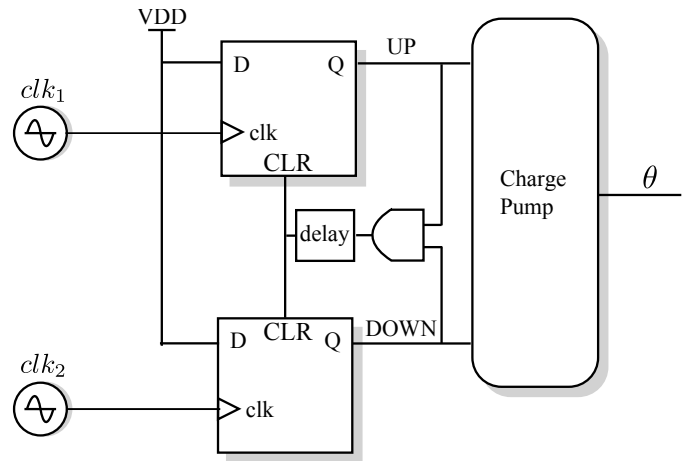

Fig. 1. Common Phase Frequency Detector

the probability that the CLR signals is acted on both flip-flops with success.

An active UP output indicates a command to increase the frequency since the clock signal clk_2 is lagging behind the signal clk_1. An active DOWN output give indicates the opposite. Therefore, UP or DOWN active outputs give the direction of phase error.

In most cases the PFD drives a charge pump; an electronic switch that dispenses a charge proportional the phase error, that in turn is fed into the loop filter on each cycle of phase comparison. Such switches require a finite time to turn on and off. If the UP and DOWN on-intervals are too short - which in the case when the phase error is low - the charge-pump switches may never turn on at all. The undetectable small phase range is called the dead-zone. The size of the dead-zone will influence the effective sensitivity of a PFD. This is a key design issue for a PFD. When the delay and reset times are large, a PFD will not be able to detect small phase error.

A feedback loop with a dead-zone is never able to settle to a firm equilibrium. Instead, it wanders continuously around the dead-zone. Wandering shows up as noise causing unwanted

and unfilterable phase noise modulation. Furthermore, the dead zone is a nonlinearity that causes inter modulation among noise components that might be present at the PFD [1]. To obviate the worst effects of a dead-zone, it is common practice to design sufficient delay into the PFD to make both D flip-flops to turn on long enough so that both charge pump switches are forced to be on simultaneously during each cycle.

There are several papers showing that by adding more elements to the presented phase frequency detector can reduce the dead-zone and with this increase the accuracy of the phase measurement [2] [3].

The purpose of our work is to present a design of phase frequency detector implemented in a digital form and able to measure phase with sub-picosecond accuracy without the use of the charge pump module, without dead zone and with a full scale linear behavior.

This paper describes in section II the digital implementation of the DMTD [4]. It aims to make frequency and phase measurements with sub-picosecond accuracy. We will also enumerate some advantages and disadvantages of the DMTD. In Section III, the performance of the presented phase frequency detector is evaluated with laboratory experiments. Finally, some conclusions are given in Section IV.

II. DIGITAL DUAL MIXER TIME DIFFERENCE

The goal of the DMTD consists in converting a phase shift from the high frequency domain into the low frequency domain, thus providing a very large time difference multiplication effect. When properly implemented, this time multiplication system allows the measurement of the short term frequency stability of two synchronous or quasi synchronous oscillators with an ultra-low background noise. It is also commonly used to measure the phase difference between two clock signals that have nearly equal frequencies, i.e., frequencies within a few hertz of one another . This technique has the benefit of cancelling most of the common clock phase noise [5].
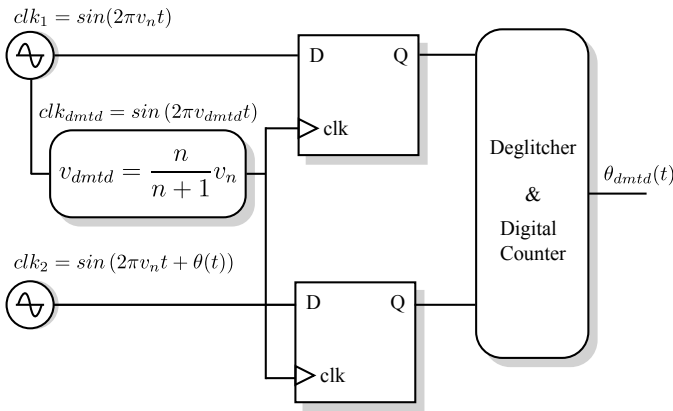
Fig. 2. Digital DMTD Schematic

A block diagram of the digital dual mixer time difference system is shown in Fig. 2. The digital DMTD consists of two D flip-flops, which act as multipliers; the D input of one of

the flip-flops is connected to a timing signal, clk_1, while the other D input is connected to the second timing signal, clk_2.

The clock input of both flip-flops is connected to a common clock source that has a frequency offset by few Hz from the clocks clk_1 and clk_2 in order to provide two low frequency beat-notes. This flip-flop clock input signal is referred to as clk_{dmtd}. The absolute frequency difference between clk_1 and clk_{dmtd} represents the system's beat frequency, clk_{beat}, which rules the overall performance of the DMTD.

$$v_{beat} = |v_n - v_{dmtd}| \tag{1}$$

The smaller the beat frequency clk_{beat} the small is the DMTD's time step τ_{dmtd}, shown in Fig. 3. The DMTD's time step τ_{dmtd} in the amount of time the transitions of the clk_{dmtd} move away from the timing signals transitions clk_1 or clk_2.

The larger the desynchronization between the clock signals clk_1 and clk_2 the larger the undesired noise contribution of the common clock [5]. Consequently, the DMTD system is appropriate for short-term measurements but not for long-term measurements if clk_2 and clk_1 do not remain quasi synchronous.
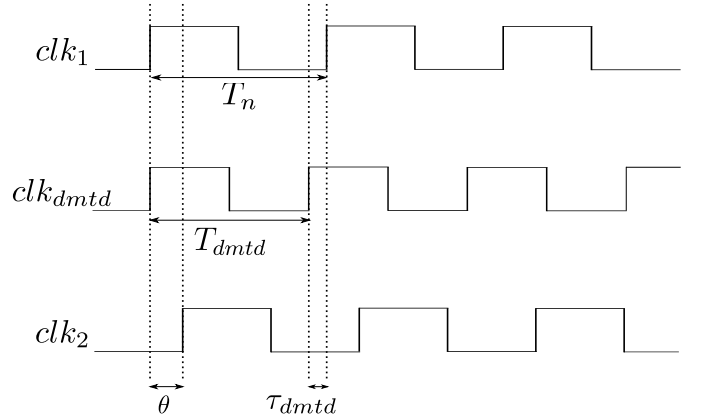
Fig. 3. DMTD's input signals

Measuring the time difference between the positive transitions of both the flip-flop output, the phase difference between the timing signal clk_1 and clk_2 is measured, but with a precision which has been amplified by the ratio of the carrier frequency to the beat frequency (over that normally achievable with this same time interval counter). The relationship between the measured time difference and the phase difference between clk_1 and clk_2 is defined by eq. 2.

$$\Delta\varphi = 2\pi\Delta t_{dmtd} \times \frac{1}{T_{beat}} \tag{2}$$

where $\Delta\varphi$ is the phase between clk_1 and clk_2, Δt_{dmtd} is the time difference between the edge transition of the flip-flop outputs and T_{beat} is the dmtd beat period as depicted in Fig. 4.

The measurement precision is such that one can measure essentially all frequency timing signals. For example, if the clock signals are at centered at 125 MHz, the beat frequencies
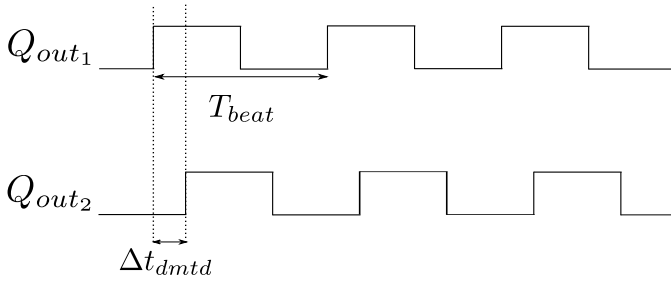
Fig. 4. DMTD's Output signals

is at 10 kHz and the time interval counter employed has a accuracy of 1 ns, then the potential measurement precision is of 80 ps, following equation 3.

$$\delta_{dmtd} = \frac{v_{beat}}{v_n} \times \delta_c \qquad (3)$$

where δ_{dmtd} is the measurement precision, v_{beat} and v_n are the beat frequency and the timing signal frequency under test respectively and δ_c is the accuracy of the counter employed.

Some of the advantages of the Digital DMTD are:

- The time counter is relatively inexpensive.
- Phase measurement with femtosecond accuracy.
- No analog parts necessary, except for the DMTD PLL which are available in many FPGA's

Some disadvantages are:

- The two oscillators need to be locked in frequency, or the phase between the oscillators tend to me move progressively apart over time.
- Very sensitive to phase noise

The described phase frequency detector does not require the use of the charge pump or a digital high speed counter to measure the time difference. It does not have a dead zone. Experiments were conducted to measure the performance of the DMTD in real time operation with clock signals having different phase noise figures. The measurements allow us to optimize some factors like DMTD frequency offset and time counter resolution against timing signals phase noise.

A. Application

The White Rabbit is a collaborative project being carried by several academic institutes as well as some industrial companies. Its objective is to use Ethernet as a synchronization network able to synchronize up to 1000 nodes with sub-nanosecond accuracy [6].

The digital DMTD presented in this paper is part of the White Rabbit ecosystem. It measures phase difference between the recovered clock and the transmitter clock and applies the correct compensation by one of two ways: one is by directly changing the phase of the transmitter clock and the other consists in directly informing the IEEE 1588 stack about the correction to apply to its clock. The place of the DMTD in the White Rabbit eco system is shown in Fig. 5. The accuracy of the White Rabbit network is measured by analyzing the Pulse Per Second (PPS) output present at each node. The result
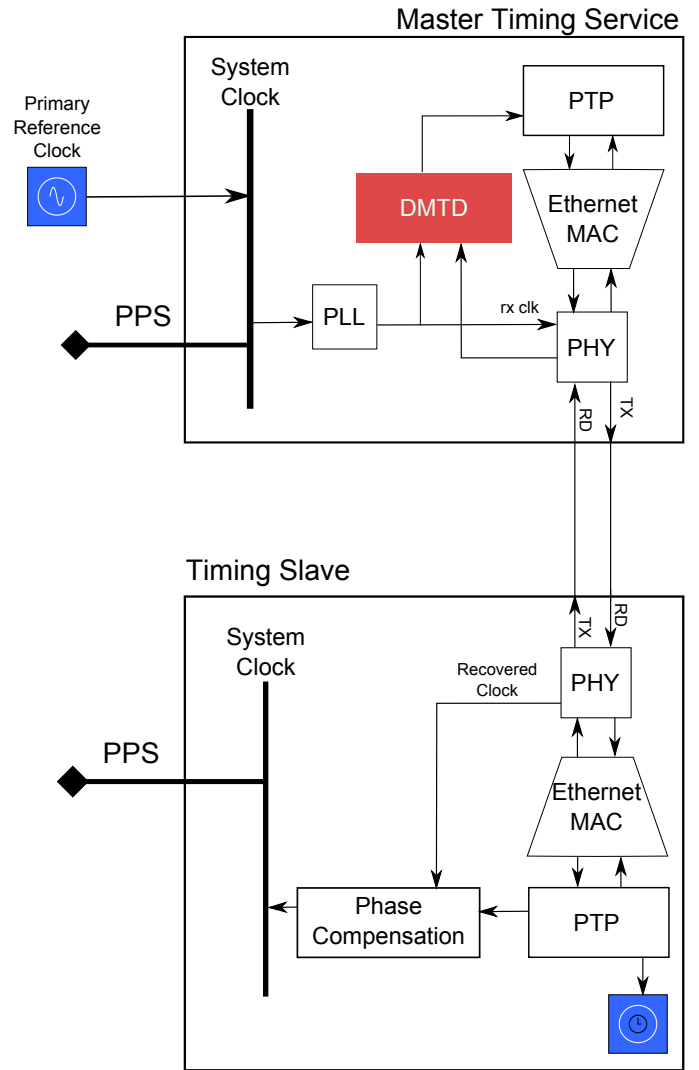

Fig. 5. White Rabbit Block Diagram

is a clock with sub-nanosecond accuracy and minimal phase accumulation between nodes.

III. MEASUREMENTS

The experimental results described in this section are supported by hardware measurements. The digital DMTD presented above was implemented in a Xilinx Spartan-6 FPGA. This FPGA has built-in PLLs (Phase-Locked Loop) and DCMs (Digital Clock Manager) with variable phase shift. Both PLLs and DCMs have different phase noise figures which allow the analysis of the DMTD behavior having different phase noise characteristics on its input timing signals.

The phase noise figures of both PLLs and DCMs were measured using the Agilent E5052A Signal Source Analyzer and are depicted in Fig. 6.

In the scope of the White Rabbit application for the implementation of the DMTD it was chosen to have a timing signal centered at 125 MHz, which represents the frequency of the recovery clock from a Gigabit Ethernet (GbE) Link.
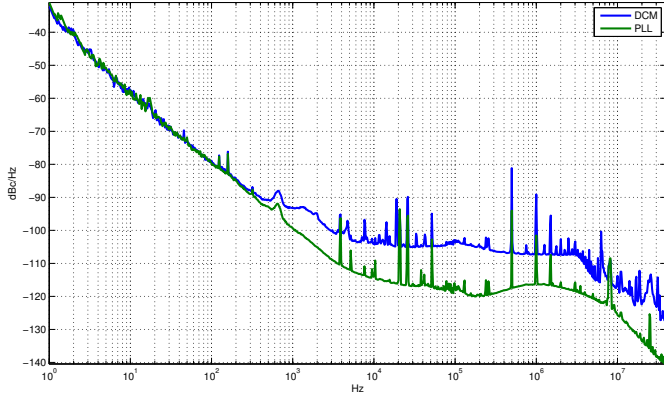
Fig. 6.   Phase Noise - Input Timing Signals

Fig. 7.   Phase Measurement (PLL)

Fig. 8.   Phase Measurement (DCM)

From the phase noise characteristics shown in Fig. 6, it is possible to estimate the jitter of the timing signals by integrating its phase noise figures. The estimated jitter J_{rms} of the PLLs is approximately 34 ps while the DCM's jitter is approximately 43 ps.

Fig. 7 shows the measured output of both flip-flops with a v_{beat} = 100 Hz, the digital counter has frequency of 125 MHz. This figure shows glitches which are due to the intrinsic phase noise present in the input timing signals. Due to the presence of glitches it is necessary to add at the output of the digital DMTD a block that filters the glitches and estimates the optimal edge transition. The deglitcher block shown in Fig. 2 is designed to choose the best edge transition in the middle of all the glitches. A straightforward and simple method would be to select the first edge, or glitch, that occurs in the output of the flip-flop. However the optimal method is to find the middle of the glitches time width and used it as the optimal edge transition. This will improve the accuracy of the phase estimation at the expense of increasing the hardware design complexity.

The measured time difference between the positive transitions, represented as Δ_{dmtd}, for a v_{beat} = 100 Hz is of approximately 640 μs, equivalent to a phase of 23°, which is a time difference of 480 ps on the timing signals at the nominal frequency. With this v_{beat} frequency, and with the digital counter with a frequency of 125 MHz we are able to measure accuracies down to 6.4 fs.

Fig. 8 shows the measured DMTD's output with a beat frequency v_{beat} = 100 Hz. However, in this case the timing signal is generated trough a DCM that has a worse phase noise figures, i.e. has more jitter. As it is shown in Fig. 8, the time width of the glitches increased, as expected. As a matter of fact by measuring the glitches time width it is possible to have a good estimation of the jitter of the input timing signal. The measured time width of the glitches is approximately 313 μs which is equivalent of having a 250 ps jitter in the timing signals.

The desglitcher block, already discussed above, removes the glitches and find the optimal edge transition by averaging the glitches time width.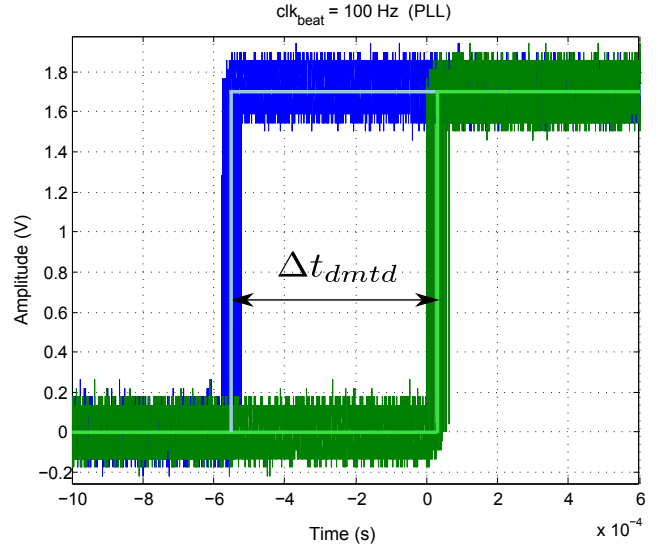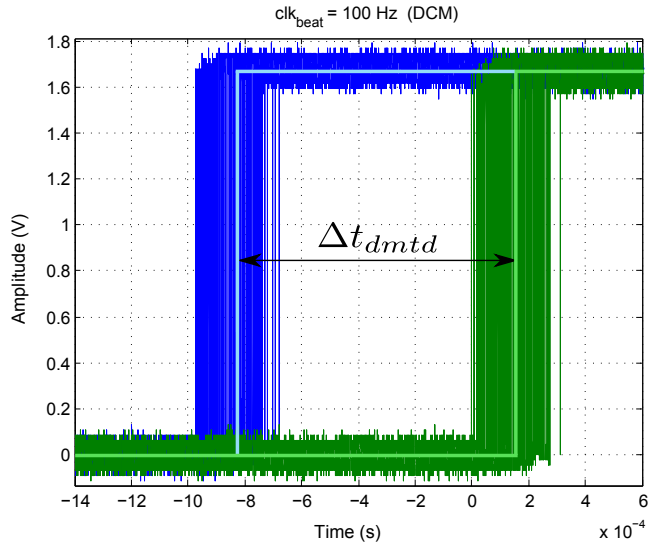 The measured time difference mean value for this presented case is approximately 980 μs equivalent to a phase measurement of approximately 35°.

Table I shows the evolution of the glitches time width and the time differences measured with different v_{beat} frequencies.

It is important to notice a behavior inherent with this type of digital design, which is observed during the edge transition of the clk_{dmtd}. This behavior is due to transition slips in the positive edge transitions of the clk_{dmtd}. The transition slips are due to the presence of jitter in the frequency of the timing signals.

In both Fig. 9 and 10 the measured frequency and time difference for a beat frequency of 1 MHz are shown respectively. This frequency has been chosen due to the fact that at this beat frequency there are no longer glitches and measurement of time difference and frequency is therefore simpler.

TABLE I

DMTD PERFORMANCE (PLL)

Beat Frequency (Hz)	$\triangle_{dmtd}$ (°)	Glitches (s)
100	23.05	30e-6
1000	23.74	4.71e-6
10 k	23.21	90e-9
100 k	24.75	0
1 M	25.53	0

TABLE II

DMTD PERFORMANCE (DCM)

Beat Frequency (Hz)	$\triangle_{dmtd}{}^\circ$	Glitches (s)
100	35.34	31.24 e-6
1000	32.03	35.57 e-6
10 k	36.15	120e-9
100 k	38.01	80e-9
1 M	40.14	0

Fig. 10.   Phase Measurement

Fig. 9 shows a beat frequency centered at 1 MHz with spurs multiples of 8 kHz. The spurs occur due to transition slips of the clk_{dmtd} and the timing signals under measurement (clk_1 or clk_2).

By analyzing both figures it is easily observed that the spurs occur with a probability that follows a Gaussian like distribution, which means that by averaging both time differences and frequency measurements we are able to find the best estimation for this parameter.

IV. CONCLUSIONS

We have shown a digital architecture for the dual mixer time difference, it was the advantages over other phase frequency detector of having a full linear scale, the measurement can be done directly from a relative low frequency counter without any analog parts. This module phase accuracy its limited by the phase noise present in all timing signals due to the presence
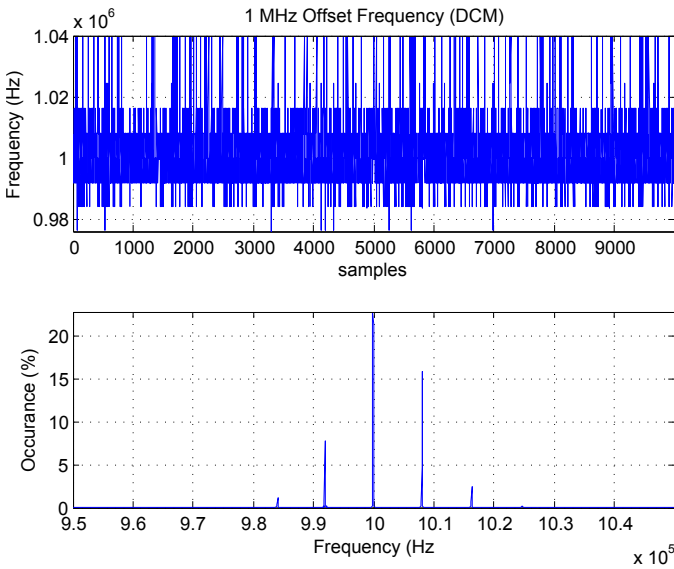
of glitches in the output of the flip-flops.
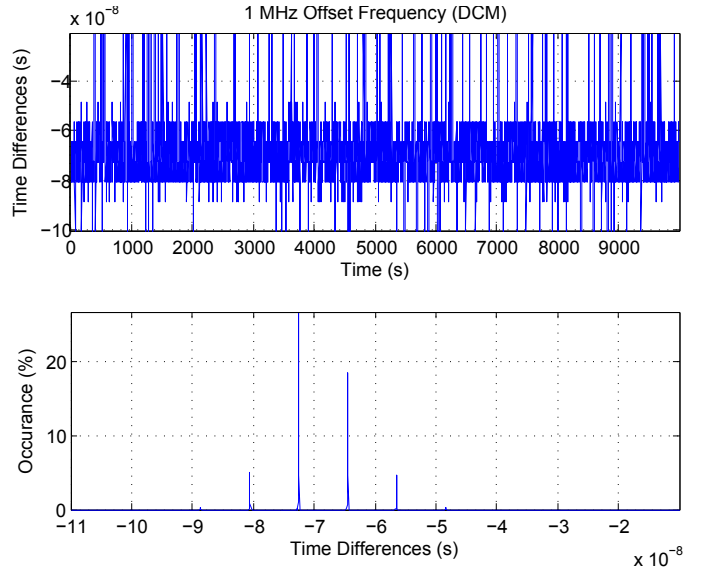
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Fig. 9.   Phase Measurement